IN THE ABSTRACT:

Please amend the abstract as follows:

"After an instruction loads data into a register at a first time, the register is monitored to see if it is read in a next clock cycle. When the data is not read in [a] the next clock cycle, the instruction is classified as a slowable instruction. An instruction address associated with the instruction is used to update a history table. The history table stores information to indicate if an instruction is a slowable instruction or a non-slowable instruction. When the instruction address of the instruction is encountered at a second time, the history table is used to determine if the instruction is slowable or non-slowable."

IN THE SPECIFICATION:

Please amend paragraph 21 as follows:

"The sequence of instruction indicates that the register R5 is loaded with data by the second instruction 110, and the same data is accessed from the register R5 immediately by the third or next instruction 115. On the contrary, even though the register R4 is loaded with data by the first instruction 105, that same data is not accessed until the fourth instruction 120 is executed. As such, the first instruction 105 does not have to be executed immediately. The data in the register R4 may be ready at any time before the execution of the fourth instruction 120 without affecting behavior of the above sequence of instructions. In addition, there may be other instructions between the first instruction 105 and the fourth instruction 120 which do not access the data in the register R4. Thus, the first instruction 105 is considered to be a slowable instruction, and the second instruction 110 is not considered to be a slowable instruction. "